IN THE CLAIMS

Claims 1-16 are cancelled.

Insert the following new claims

17. (New) A process for forming a contact for a semiconductor device comprising:

forming a first compound semiconductor layer, wherein the first compound semiconductor material layer includes a first compound semiconductor material and has a first conductivity type dopant;

forming a second compound semiconductor layer on the first semiconductor layer, wherein the second compound semiconductor layer includes a second compound semiconductor material and has a second conductivity type dopant and the second conductivity type is opposite the first conductivity type;

forming a third compound semiconductor layer on the second compound semiconductor layer, said third compound semiconductor layer of said first conductivity type dopant, wherein the first, second and third layers are active layers in a transistor device;

patterning the third compound semiconductor layer to define an opening therein with a wall, said opening exposing a portion of the second active layer; and

forming a fourth compound semiconductor material upon at least a portion of the exposed second active compound semiconductor layer wherein the fourth compound semiconductor material has the second conductivity type dopant and has a dopant concentration that is higher than the dopant concentration of the second compound semiconductor layer;

depositing a planar layer of insulating material and patterning the planar layer of insulating material to have contact openings over the third and fourth layer; and

forming contacts in the openings in the planar layer of insulating material from the surface of the planar layer to the third layer and through the fourth layer to the underlying second layer in order to provide a substantially common plane for the upper surfaces of the contacts to the third and second layers.

18. (New) The process of claim 17, wherein the fourth compound semiconductor material is formed by sputtering.

19. (New) The process of claim 17, wherein each of the first, second, third and fourth compound semiconductor materials include at least two Group IVA elements.

20. (New) The process of claim 17, wherein each of the first, second, third and fourth compound semiconductor materials include silicon carbide.

21. (New) The process of claim 17, further comprising forming a first metal contact of a first type of metal on the third semiconductor layer and forming a second metal contact of a second type of metal on the fourth semiconductor layer.

22. (New) The process of claim 21, wherein an electrical connection between the third compound semiconductor material and the first metal layer is ohmic and an electrical connection between the fourth compound semiconductor and the second metal layer is ohmic.

23. (New) The process of claim 21, wherein the first metal layer comprises aluminum and the second metal layer comprises nickel.

24. (New) A semiconductor device comprising:

a first active layer including a first compound semiconductor material and having a first conductivity type dopant;

a second active layer including a second compound semiconductor material and having a second conductivity type dopant opposite the first conductivity type, wherein the second active layer contacts the first active layer;

a third active layer including a third compound semiconductor material and having the first conductivity type dopant, wherein the third active layer contacts the second active layer, and a combination of the first, second, and third active layer are at least part of a transistor;

an opening defined by said second and third active layers, said opening extending through the third active layer, said opening contacting and terminating within the second active layer;

one or more sidewall insulating layers within the opening to isolate the opening from the adjacent third layer

a fourth compound semiconductor material at least partially within the opening and on the second active layer, wherein the fourth compound semiconductor material has the second conductivity type dopant and a dopant concentration higher than the dopant concentration of the second active layer and is electrically connected to the second active layer; and

a planar layer of insulating material on the third layer and over the fourth layer and comprising first and second sets of metal contacts, said contacts separated from each other by said insulating material layer with one set of metal contacts in electrical contact with the third layer, the other set of contacts in electrical contact with the fourth layer, wherein upper surfaces of the metal contacts and the planar layer lie in substantially the same plane.

25. (New) The device of claim 24, where each of the first, second, third, and fourth compound semiconductor material include at least two Group IVA elements.

26. (New) The device of claim 24, where the first, second, third, and fourth compound semiconductor material comprise silicon carbide.

27. (New) The device of claim 24, further comprising electrical contacts to the third active layer and the fourth compound semiconductor material.

28. (New) The device of claim 27, wherein the metal layers are aluminum and nickel, respectively, and the electrical contacts are ohmic.

29. (New) The device of claim 28, wherein the device further comprises a second insulating layer on the surface of the third active.

30. (New) The device of claim 24, wherein the second active layer has a thickness in a range of approximately 0.1 - 2 microns thick.